GaAs/GaAlAs BIPOLAR HETEROJUNCTION GATE ARRAY

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Several technological issues related to the development of GaAs bipolar heterojunction gate arrays were investigated experimentally using a test bar design that consists of discrete transistors, three types of HI^2L gates, and a prototype gate array with 114 internal gates and 25 I/O buffers. The preparation of submicrometer epitaxial films composed of AlGaAs and GaAs layers required for this development were also examined. Two methods of growing epitaxial films, OMCVD and MBE,

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were evaluated. It was concluded that although MBE is a slow process it is superior to OMCVD in providing uniform epitaxial films with controlled doping concentrations over large area wafers.

Two sources of MBE material, one from the University of Illinois, Urbana, Illinois and another from the Materials Science Laboratory of Texas Instruments, were used to examine the relationship between material and transistor current gain. For an inverted transistor structure required for an HI^2L gate, it was found that lower aluminum composition and higher donor concentration in the AlGaAs buried emitter tend to yield higher current gain. Moreover, transistors fabricated by ion implanted junctions tend to have higher current gain than those fabricated by epitaxial grown junctions.

The basic HI^2L gate using nominal 3 μm design rules was characterized by ring oscillators and D-type divider circuits. At V_{cc} = 2 V and power dissipation of 2.0 mW per stage, the measured propagation delay was 270 ps for fan-out of 1 and 470 ps for fan-out of 4. Toggle frequency as high as 200 MHz was also applied successfully to a divide by 4 circuit using this technology.

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SECTION I
INTRODUCTION

This interim report describes the results of a GaAs/GaAlAs bipolar heterojunction gate program, sponsored by the Defense Advanced Research Projects Agency and monitored by the Office of Naval Research under Contract No. N00014-82-C-0212. The objective was to develop a technological base for the design and fabrication of GaAs bipolar heterojunction gate arrays having a density of 4000 gates per chip, and evaluate their performance, yield, and reliability by a family of medium scale (< 100 gates) logic circuits implemented on the gate arrays. The technical monitor of this development program is Dr. Ken Davis. This report covers the first year effort from February 1, 1982 to January 31, 1983.

The major activities in this period were:

- Compare the results of an organometallic chemical vapor phase epitaxial technique (OMCVD) to a molecular beam epitaxial technique (MBE) to provide thin (< 1 μm) uniform multi-epitaxial layers composed of GaAs and GaAlAs on 5 cm diameter GaAs substrates.

- Develop a high yield process consisting of ion implanted bipolar transistors, reliable ohmic contacts, and two level metal interconnections so that large scale gate arrays can be fabricated.

- Characterize GaAs bipolar transistors to understand the effects of MBE growth materials on transistor current gain and switching speed.

- Design and fabricate a prototype HI^2L gate array with 114 internal gates and 25 I/O buffers.

SECTION II
MATERIAL DEVELOPMENT

A. Organometallic CVD (OMCVD)

Heterojunction bipolar gate arrays require multilayer structures with tight control of doping, band gap, and thickness. Base layer thickness uniformity of approximately 10% is necessary to obtain a uniform current gain across the wafer. The desired wafers are round, with a diameter of two, and eventually three inches. These requirements call for a large rotating substrate holder and a true cold wall reactor system. Such a system, so far, can only be implemented by using arsine as the arsenic source. Because of the extremely poisonous property of arsine, it is generally not acceptable in an ordinary manufacturing area. Therefore at the outset of this program, we took two rather unconventional approaches and hoped that they could solve the arsenic source problem.

The first unconventional approach is to replace arsine with trimethylarsenic as the arsenic source. The second unconventional approach is to use lamp heat through the reactor wall, and rely on optical mirrors to prevent premature cracking of the organometallic compounds.

An experimental OMCVD system designed to examine the feasibility of the alternative approaches was constructed. The system, shown in Figure 1, features a horizontal tube and a radiation-heated graphite susceptor. It is designed for operation under atmosphere pressure. The organometallic source materials are trimethyl gallium (TMGa) and trimethyl arsenic (TMAs). The TMAs is a liquid with a vapor pressure similar to that of TMGa (~ 200 Torr at room temperature) and is being handled in steel bottles like TMGa.

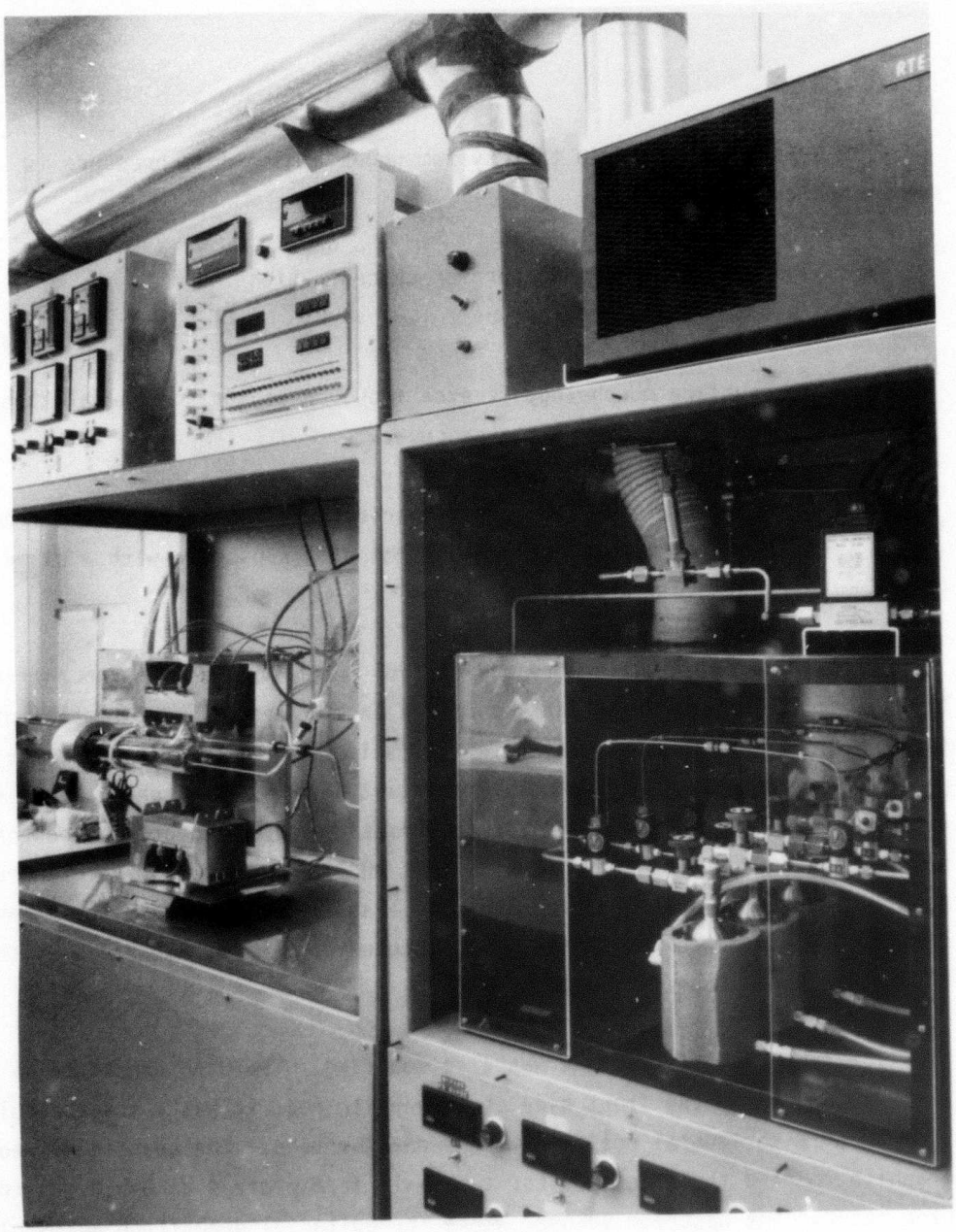


Figure 1 Photograph of the OMCVD System. It features a horizontal tube and a radiation-heated graphite susceptor.

The GaAs layer grown in this system under atmospheric pressure is summarized as follows:

- The lowest background carrier concentration found is $n \sim 1 \times 10^{17}$ cm^{-3} (n-type).
- The surface morphology is excellent. Best surfaces equal those grown by the established $AsCl_3$ process.
- The epitaxial layer thickness varies by a factor of 2 to 3 from the upstream to the downstream portion of a substrate with a diameter of approximately 5 cm.

To improve layer uniformity and control background doping concentration, the gas manifold was subsequently modified in two ways. The formation of a deposit was observed at the point in the manifold where the TMAs and the TMGa gases mix. This deposit is probably a TMGa-TMAs adduct, which is known to have a low vapor pressure. To avoid adduct formation, the reactor tube now has two separate gas inlet tubes, one for the TMAs and the second for the other organometallic compounds. In addition, the gas lines downstream from the organometallic bubblers are now small ID glass tubes coupled by ACE vacuum fittings, to allow visual inspection.

The susceptor arrangement was also modified. The GaAs substrate is made to be supported by the front side of a graphite rod, it has a perpendicular instead of a horizontal position to the reactor tube. The spacing between the graphite rod and the inner reactor tube wall is minimized to avoid gas convection between the upstream volume, where the epitaxial deposition takes place, and the downstream volume. This design also assures that no unreacted organometallic compounds reach the downstream reactor volume.

Heating of the graphite susceptor is still accomplished by lamps. Optical mirrors prevent the radiation from reaching the upstream reactor volume so that the organometallic compound does not thermally decompose before reaching the GaAs substrate.

In the modified reactor we have observed that the background carrier concentration dropped with a reduced As-to-Ga molar ratio, which is in agreement with published literature.[1,2] The best values we obtained are:

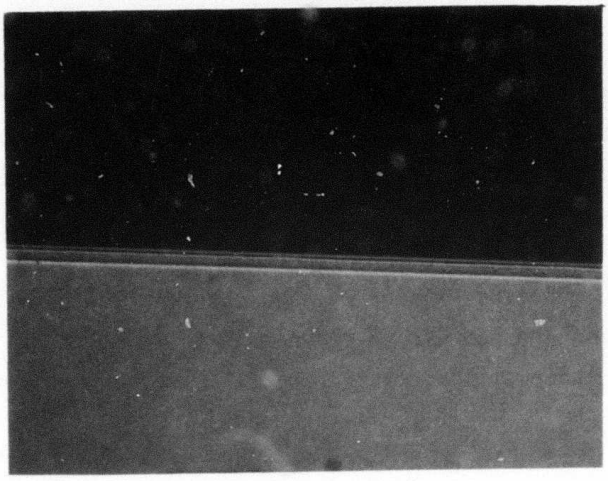
Electron concentration: $N = 3.8 \times 10^{16}$ cm^{-3}

Electron mobility: μ_n (300 K) = 5080 cm^2/V-s

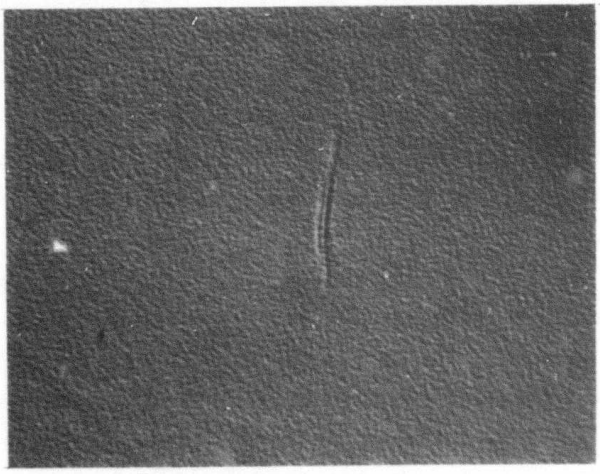
μ_n (77 K) = 6580 cm^2/V-s.

Experiments also were conducted to deposit GaAlAs epitaxial layers. The deposition conditions (temperature, gas flow rates) were by no means optimized, but several promising samples have been obtained. Figure 2(a) and (b) shows a stained cross section and a micrograph, respectively, of the surface morphology of a structure consisting of a $Ga_{0.8}Al_{0.2}As$ layer approximately 2 μm thick, followed by a 0.7 μm thick GaAs layer. Efforts to characterize the AlGaAs layer by Hall measurements were not successful because of the difficulty in making ohmic contacts on an AlGaAs layer.

With this arrangement, although we were able to grow both GaAs as well as AlGaAs layers, the background doping with acceptable surface morphology was constantly too high, in the 1×10^{17} cm^{-3} range, as opposed to less than 1×10^{16} cm^{-3} reported from the arsine based system. We had suspected that leakage in the upstream plumbing system might cause the high background doping. But repeated effort to make the plumbing system vacuum tight did not appear to solve this problem. In view of the difficulty we had encountered, we decided in December 1982 not to pursue the nonarsine based OMCVD technique further.



(a)



(b)

Figure 2(a) Cross Section of Stained GaAs/GaAlAs/Cr-GaAs Structure
(b) Nomarski Micrograph of Surface Morphology

B. Molecular Beam Epitaxy (MBE)

1. University of Illinois

At the outset of this program, a subcontract was awarded to Professor Hadis Morkoc of the Coordinated Science Laboratory of the University of Illinois at Urbana-Champaign, Illinois.

The subcontract calls for the growth of GaAlAs/GaAs heterojunction material using the University of Illinois MBE machine and a study of the current transport properties of such junctions as a part of the GaAs bipolar gate array development program. The MBE machine, a Riber MBE-1000, installed at the University of Illinois is an upgraded first generation laboratory model, in which a cryo-shroud used to getter residue gas was added to the growth chamber, but the machine was not equipped with a rotating substrate holder necessary for uniform epitaxial growth. Therefore, the machine can only grow pieces of material usually less than 2.5 cm square, to investigate the properties of discrete transistors and small circuits, for example, ring oscillators and divide-by-2 circuits. During the period covered by this report, the University of Illinois grew a total of 20 such MBE wafers for the program. The epitaxial layers of these wafers and the resultant transistor characteristics fabricated on these materials are described in Section III.B. In general, two types of materials were prepared. One type had a 1.0 μm n^+ $Al_xGa_{1-x}As$ layer followed by a 0.5 μm n^- GaAs layer grown on n^+ GaAs substrates. Another type had the same 1.0 μm n^+ $Al_xGa_{1-x}As$ layer, but instead of the n^- GaAs layer, a 0.2 μm p-type GaAs layer with $N_A = 1 \times 10^{18}$ cm^{-3} and a 0.3 μm n-type GaAs layer with $N_D = 2 \times 10^{17}$ cm^{-3} were grown on top of $Al_xGa_{1-x}As$ layer. The former was used to study the property of implant junction transistors and the latter was used to study the property of grown junction transistors.

2. Texas Instruments

A second generation Riber MBE-2300 machine (see Figure 3) was installed in March 1982 in the Materials Science Laboratory of Texas Instruments Incorporated. This machine is similar to the machine at the University of

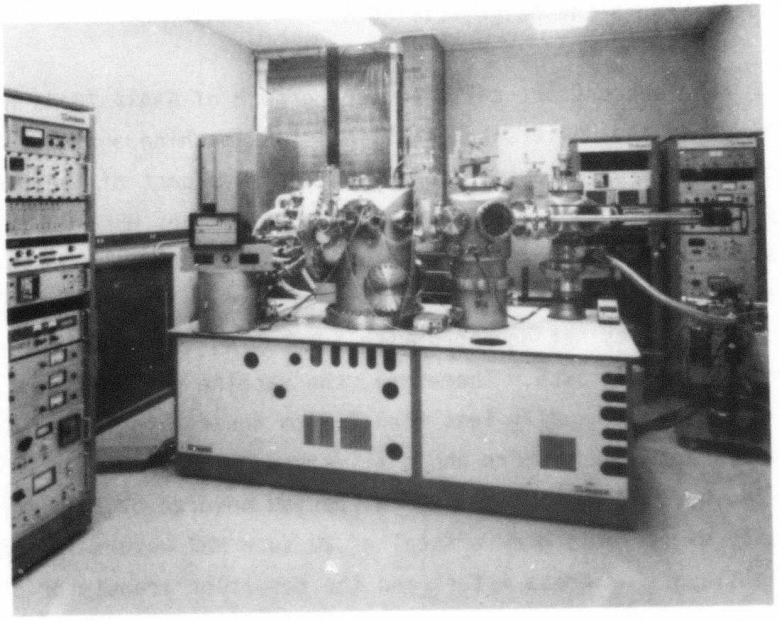


Figure 3 The Riber MBE-2300 Machine Installed in the Materials Science Laboratory of Texas Instruments Incorporated.

University of Illinois. But in addition to the cryo-shroud, the machine was also equipped with a rotating substrate holder that can handle wafers as large as 5 cm in diameter. A GaAs layer with excellent mobility and thickness uniformity over an entire 5 cm substrate was grown successfully two months after installation. The first attempt to grow $Al_xGa_{1-x}As$ was started in August. From that time until the end of January 1983, a total of nine wafers, all intended for developing grown junction structures, were supplied for transistor fabrication. The characteristics of these transistors are presented in Section III.B.

C. Ion Implant

During this program phase, one of the major materials development objectives has been to establish a reproducible p-type doping technology using ion implantation. Be was chosen over Mg for most of our implantation/annealing experiments because of its range advantage for implanting deep channels such as those required for the p-type base region of the bipolar transistor. The first experiment to be carried out was to measure the atomic profiles of Be implants before and after annealing using the Secondary Ion Mass Spectroscopy (SIMS) facility in TI's Materials Science Laboratory. Figures 4(a) and (b) show the results. These atomic profiles clearly establish the non-Gaussian doping behavior of Be during annealing.

Several experiments were then carried out to examine the effect of implant conditions on the profiles. First, coimplants of Be plus As, and Be plus C were examined. The contribution of planar channeling to the observed profiles was also investigated by comparing Be implanted with the off-axis tilt direction toward the (110) vs tilting toward the (100). All subsequent anneals were carried out at 700°C for 15 minutes using arsenic overpressure in addition to a proximity cover slice. However, no improvement was observed in the profiles for any of the Be experiments. Conditions were also investigated to minimize the time and temperature used in Be annealing. Annealing conditions, no matter how minimal (e.g., 500°C for 15 minutes), which activate Be, were found to yield non-Gaussian profiles.

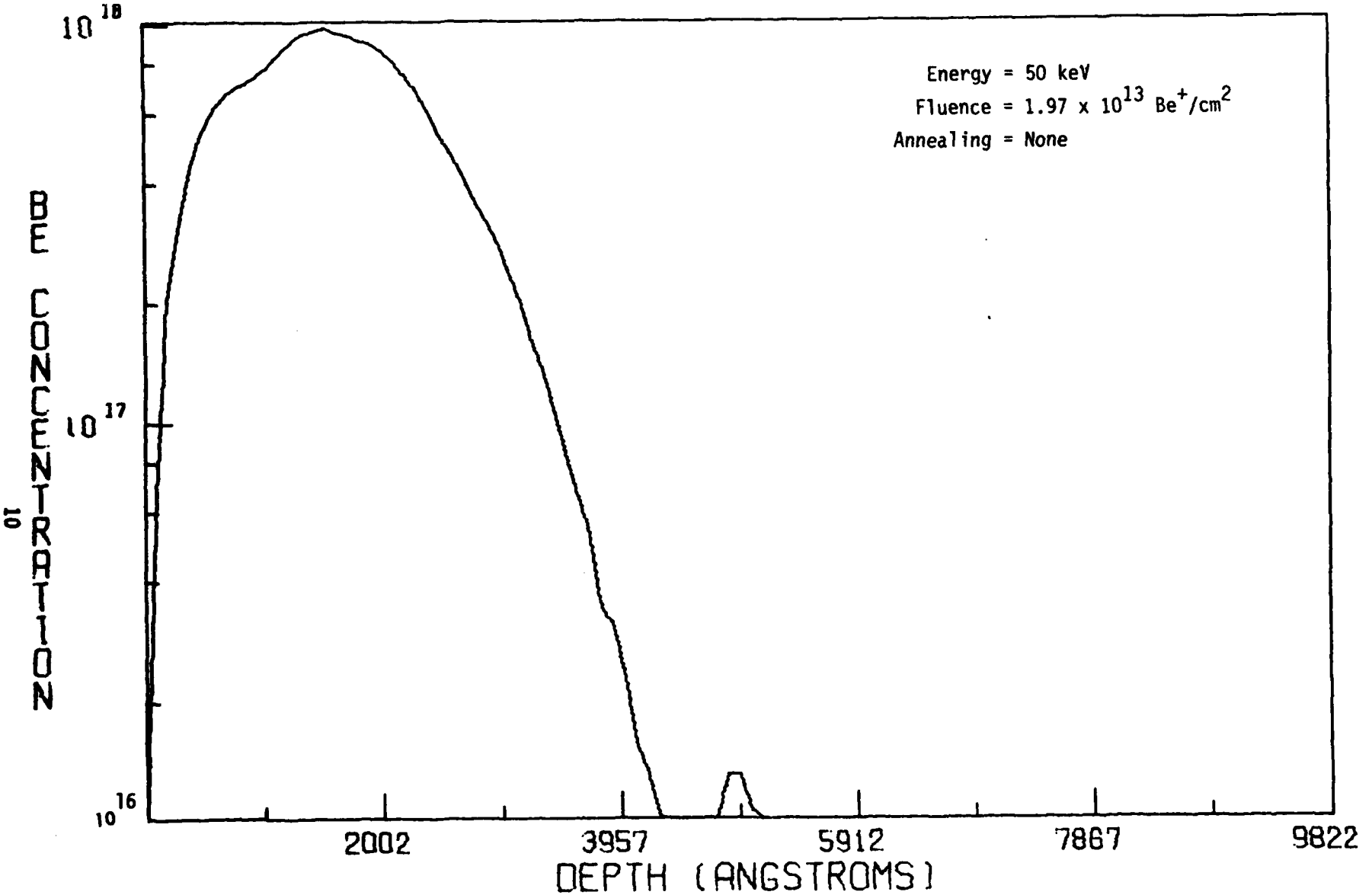


Figure 4(a) SIMS Profile of Be Implant Before Annealing

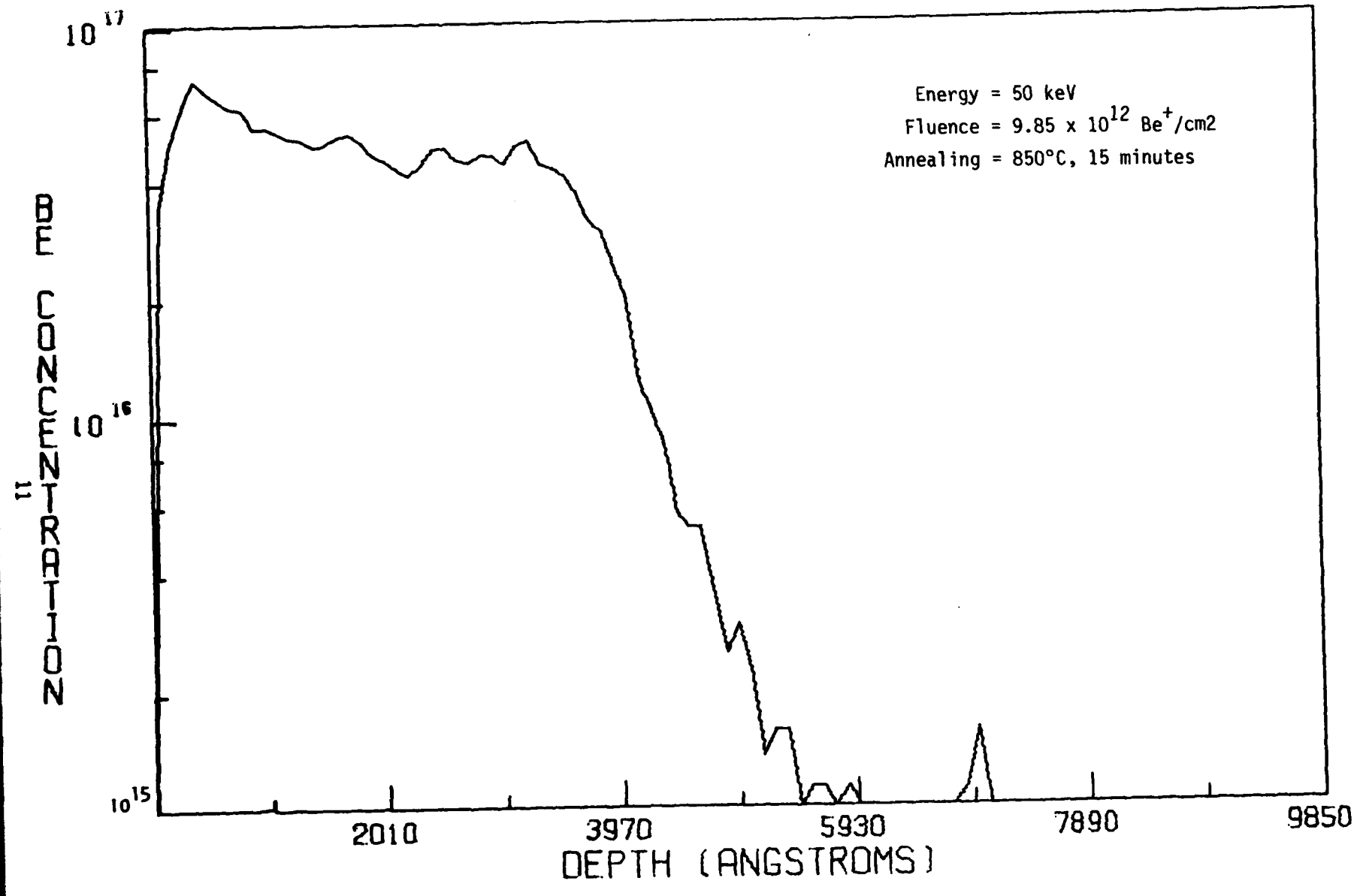


Figure 4(b) SIMS Profile After Annealing

Although there have been no major difficulties in applying non-Gaussian Be profiles for heterojunction bipolar ICs, one troublesome aspect still remains. The electrical activation efficiency of the p-type beryllium implant, as determined by C-V measurements, has consistently been only 50 to 60%. This is in contrast to several reports in the literature indicating 80 to 100% activation, as determined by Hall measurements.[3-5]

To resolve the discrepancy a split lot experiment was performed in conjunction with the University of Illinois to check for problems with beam purity in TI's Extrion ion implanter and differences caused by annealing with a Si_3N_4 encapsulant.

No differences were observed in the C-V profiles for slices implanted in TI's Extrion implanter and in the University of Illinois implanter. Identical profiles were also observed for 850°C arsenic overpressure annealing and Si_3N_4-encapsulated annealing. The electrical activation efficiency was still only 50 to 60%, as observed in earlier studies.

Thus we surmised that the results found in the literature may result from Hall effect measurements using a Hall factor of unity. The Hall factor is not well known for GaAs, and to our knowledge has never been measured for either ion-implanted or p-type material. Implantation-induced defects may significantly alter the scattering mechanisms that determine the Hall factor. Measurements of the Hall factor on n-type GaAs[6] have typically ranged from 1.0 to 1.2; consequently, a unity Hall factor could cause an overestimate in the electrical carrier concentration by as much as 20%.

SECTION III
PROCESS DEVELOPMENT

A. Baseline Process

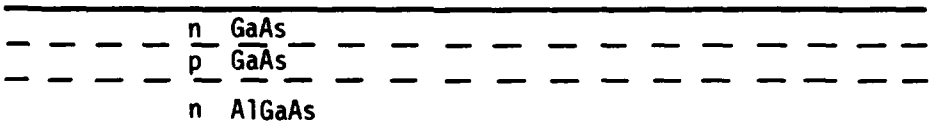
Several improvements have been made in the baseline process since the start of the bipolar heterojunction gate array program. The more important process changes to improve the fabrication include the use of depletion MESFET loads instead of ungated resistive loads, elimination of all p-type/n-type ohmic metal overlays, and an extra mask level to allow a higher dose p-type implant under the load to increase the punchthrough voltage.

Difficulties encountered earlier in controlling the sheet resistivity of the top n-layer necessitated the change to a depletion MESFET load instead of a resistive load. A depletion load allows the use of gate recessing to obtain the desired channel conductivity and also circumvents the surface state variability problems typical of high resistivity ungated loads. However, because of the likelihood that punchthrough occurs under the load in devices that utilize extremely thin base layers, an extra mask level was added to the new process design to allow a higher dose p-type implant under the load.

Problems were also observed occasionally with the surface morphology of the AgMn/AuGeNi ohmic contact overlay. Because the overlay could become a source of potential failure in the future, it was eliminated completely. Separate AuZn/AuGeNi ohmic contacts were used, and the contacts were butted by second-level metal.

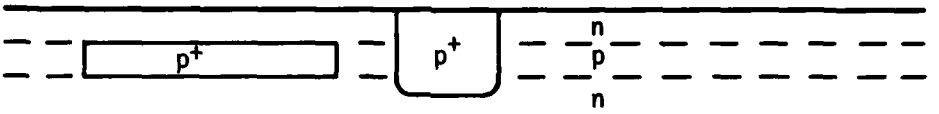
The improved fabrication sequence for the GaAs HI^2L process is illustrated in Figure 5, which shows cross-sectional views of the GaAs slice at various stages of the process. The collector and base regions can be either implanted as in the case of implant junction transistors, or grown by MBE, as in the case of grown junction transistors. The mask set presently in use consists of seven

1. Collector and Base Implants

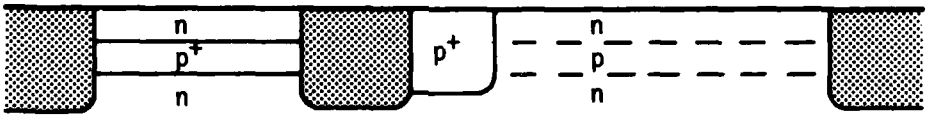


2. p^+ Load Isolation Implant

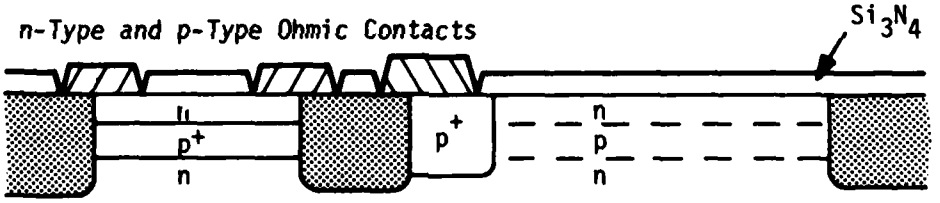
3. p^+ Contact Implant



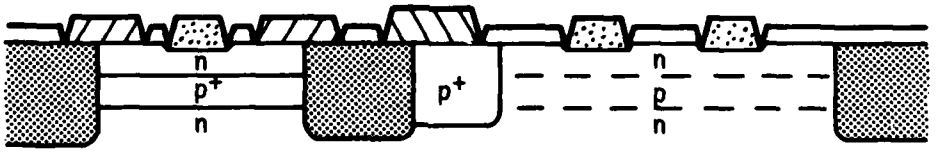
4. Boron Isolation Implant



5. *n-Type and p-Type Ohmic Contacts*



6. Recessed Schottky Contact



7. Polyimide Via and Second-Level Metal

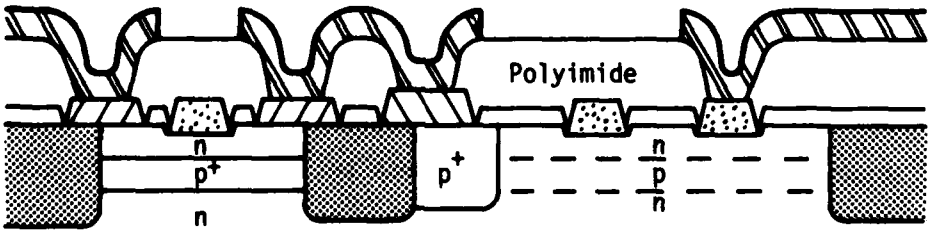


Figure 5 Process Sequence for GaAs HI^2L Gate Arrays

essential levels. Two additional levels, one for etching of alignment marks and one for enhanced load implant, are optional. The latter level was needed only when the punchthrough voltage under the load was too low, but is not currently used in our process.

B. Transistor Characteristics

1. Inverted Heterojunction Transistor

For gate array development using HI^2L technology (shown schematically in Figure 6) an inverted heterojunction transistor structure is essential. The transistor must be able to provide adequate current gain for the logic gate to function properly. Taking a fan-out = 4 HI^2L gate design as an example, a minimum current gain of 10 is required. But to insure sufficient noise margin under a variety of load and temperature conditions a current gain of 20 is more desirable.

During the first year of this program effort was devoted to develop a high current gain transistor. Twenty MBE wafers were received from the University of Illinois and nine wafers were received from the in-house MBE facility. The I-V characteristics of a high gain inverted heterojunction on a bipolar transistor are shown in Figure 7. High current gain such as this, however, was not always achievable under the same material preparation and device process conditions. Tables 1 and 2 summarize the measured transistor gain corresponding to each MBE wafer prepared by the University of Illinois and by Texas Instruments. The grown junction transistor refers to the p-type doped base of the transistor that is made out of epitaxial growth, as contrasted to the implant junction transistor that is made by Be ion implant.

Although definite conclusions regarding the large fluctuation of current gain in both implant junction and grown junction transistors are not yet possible, several trends can be seen from Tables 1 and 2.

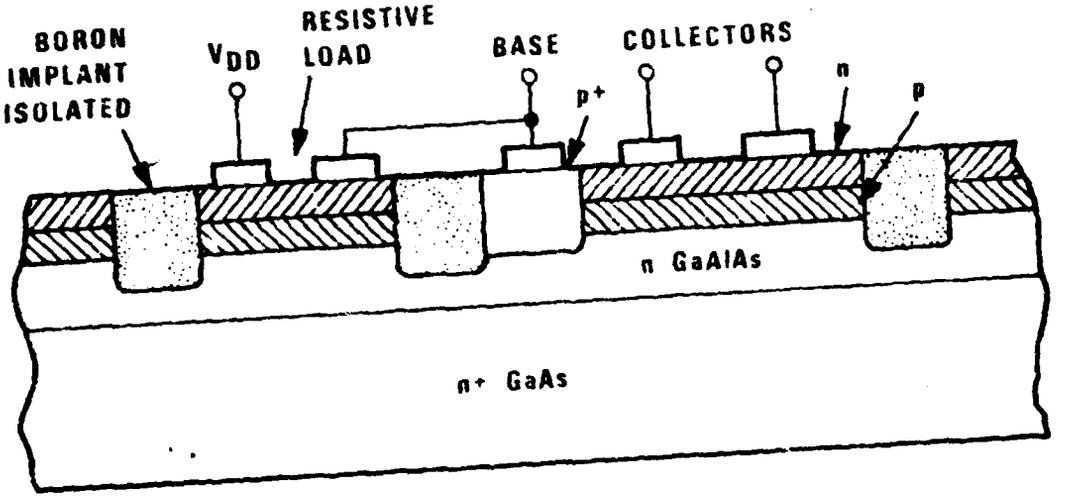


Figure 6 An Inverted Heterojunction I^2L (HI^2L) Gate Structure

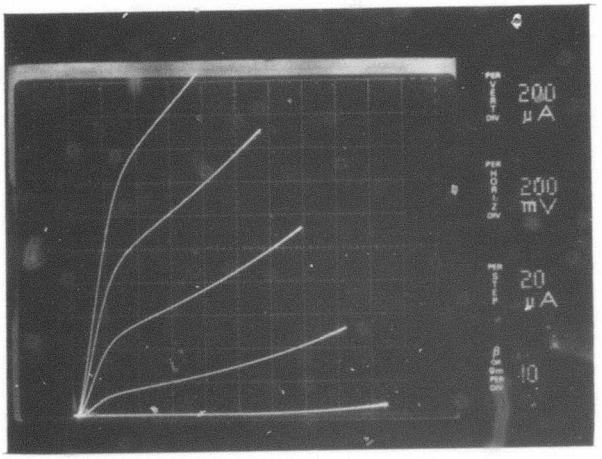


Figure 7 Typical I-V Characteristics of a High Gain Inverted Heterojunction Bipolar Transistor

Table 1

MBE Material Grown by UI

	composition (x =)	$Al_xGa_{1-x}As$ thickness (μm)	donor concentration (cm^{-3})	junction formation	h_{FE}
UI-245*	0.2	2	5×10^{18}	grown	~ 4
UI-357*	0.15	2	1×10^{18}	implant	15 ~ 100
UI-420	0.2	2	1×10^{18}	implant	8 ~ 20
UI-428	0.2	2	1×10^{18}	implant	~ 2
UI-431	0.2	2	1×10^{18}	implant	~ 2
UI-449	0.2	2	5×10^{17}	grown	4 ~ 5
UI-527	0.25	1	5×10^{17}	grown	4 ~ 6
UI-615	0.2	0.6	2×10^{17}	grown	< 1
UI-621	0.2	0.5	2×10^{17}	implant	5 ~ 40
UI-784	0.2	0.8	1×10^{18}	implant	< 1
UI-789	0.15	0.8	1×10^{17}	grown	< 1
UI-823	0.20	0.8	1×10^{18}	implant	4 ~ 6
UI-824	0.25	0.8	4×10^{17}	grown	< 1
UI-846	0.20	0.5	2×10^{17} (G)**	grown	1 ~ 2
UI-847	0.20	0.5	2×10^{17} (G)	grown	1 ~ 2
UI-845	0.20	0.5	2×10^{17} (G)	implant	0.5 ~ 2
UI-877	0.20	0.5	7×10^{17} (G)	grown	5 ~ 8
UI-879	0.30	0.5	7×10^{17} (G)	grown	10 ~ 15
UI-868	0.15	1.0	1×10^{18} (G)	implant	0.4 ~ 15
UI-869	0.15	0.5	1×10^{18} (G)	implant	0.4 ~ 15
UI-1024	0.20	1.0	5×10^{17} (G)	grown	5 ~ 25
UI-1037	0.15	1.0	5×10^{7} (G)	grown	8 ~ 30

* Materials grown before February 1, 1982

** (G) stands for Graded Heterojunction

Table 2

MBE Material Grown by TI

	composition ($Al_xGa_{1-x}As$, x ≈)	$Al_xGa_{1-x}As$ thickness (μm)	donor concentration (cm^{-3})	junction formation	h_{FE}
TI-63	0.3	0.9	1×10^{17}	grown	< 1
TI-66	0.3	1.2	1×10^{17}	grown	< 1
TI-67	0.3	1.0	1×10^{17}	grown	4 ~ 6
TI-68	0.3	1.6	5×10^{17}	grown	4 ~ 6
TI-76	0.35	1.9	5×10^{17}	grown	7 ~ 9
TI-129	0.25	1.4	5×10^{17} (G)	grown	< 1
TI-141	0.20	1.0	5×10^{17} (G)	grown	< 1
TI-142	0.18	1.1	5×10^{17} (G)	grown	~ 1
TI-144	0.20	1.4	5×10^{17} (G)	grown	< 1
TI-134	0.15	0.9	5×10^{17}	implant	20 ~ 30
TI-138	0.13	0.9	5×10^{17}	implant	20 ~ 25
TI-139	0.17	0.9	5×10^{17} (G)	implant	2 ~ 3
TI-141	0.18	1.1	5×10^{17} (G)	grown	< 1
TI-142	0.20	1.0	4×10^{17} (G)	grown	< 1

a. Implant junction in general has better current gain than grown junction. It is possible that the 850°C anneal required for silicon implants is beneficial in either annealing defects or grading the heterojunction interface to reduce the effect of the conduction band discontinuity believed to exist at abrupt heterojunctions.

b. Most of the grown junction slices utilizing $x \approx 0.3$ and processed earlier had lower current gain than slices utilizing $x = 0.15$ to 0.2 and processed later. It has recently been reported[7] that Si-doped carrier concentration in $Al_xGa_{1-x}As$ grown by MBE is extremely sensitive to aluminum composition near $x \approx 0.34$, because of high donor activation energy around the direct-indirect band crossover point.

c. An increase in donor concentration in $Al_xGa_{1-x}As$ to higher than 5×10^{17} cm^{-3} and a decrease in acceptor concentration to lower than 3×10^{17} cm^{-3} in active base improves current gain. It is possible that a higher doping in the emitter is necessary to prevent the tail of the Be base implant from migrating into the $Al_xGa_{1-x}As$ region during high temperature implant annealing.

A major source of uncertainty with the University of Illinois material has been that its MBE system lacks a rotating substrate holder. As a result, there is always a larger than a factor of two difference in both doping level and thickness across a slice. Thus detail comparison between transistor current gain and material property is difficult.

Another source of uncertainty is the lack of a simple, reliable technique to characterize the composition and doping level in $Al_xGa_{1-x}As$ and at the heterojunction interface. Among the three techniques available at TI, photoluminescence (PL), Secondary Ion Mass Sectroscopy (SIMS), and CV profiles, PL is the only practical means to measure the composition of $Al_xGa_{1-x}As$. But its accuracy appears to be greatly affected by the doping level and trap

density in the $Al_xGa_{1-x}As$ layer. SIMS can be applied to study the heterojunction, in principle, but it does not have the required spatial resolution and the calibration accuracy. And finally, CV profile can be applied to abstract the doping concentration vs depth, but it cannot be applied to inhomogeneous material composed of a multi-layer junction structure. As a result, in most experimental situations we can only compare transistor current gain to material parameters provided by MBE growth, which is not reliable either.

To solve this difficulty a program has been initiated in conjunction with Materials Science Laboratory to develop a more coherent method to characterize $Al_xGa_{1-x}As$/GaAs heterojunctions.

2. Non-Inverted Heterojunction Transistors

The properties of non-inverted heterojunction transistors grown by MBE were studied under the subcontract agreement by researchers at the University of Illinois. With a set of photomasks provided by Texas Instruments, both single and double heterojunction bipolar transistors were fabricated. Figure 8 shows a typical structure of such a transistor. The double heterojunction type is particular interesting because it has smaller turn-on saturation voltage, hence it is more suitable for logic circuit applications.

To be able to use selective etching, an AlAs mole fraction of 40%, which is much larger than the previous wafers prepared by MBE for inverted transistors, was used for such device fabrication. The need for such a high mole fraction, particularly in the bottom $Al_xGa_{1-x}As$ layer imposes stringent growth conditions; therefore, extremely optimized growth conditions were used to grow the double heterojunction bipolar junction transistors (DHBJTs). The best common emitter current gains obtained for these transistors are 1650, 850 and 500 for base widths of 100, 200, and 500 nm respectively. These results compare very favorably with the best previous value of 120 by MBE and 1600 by LPE.

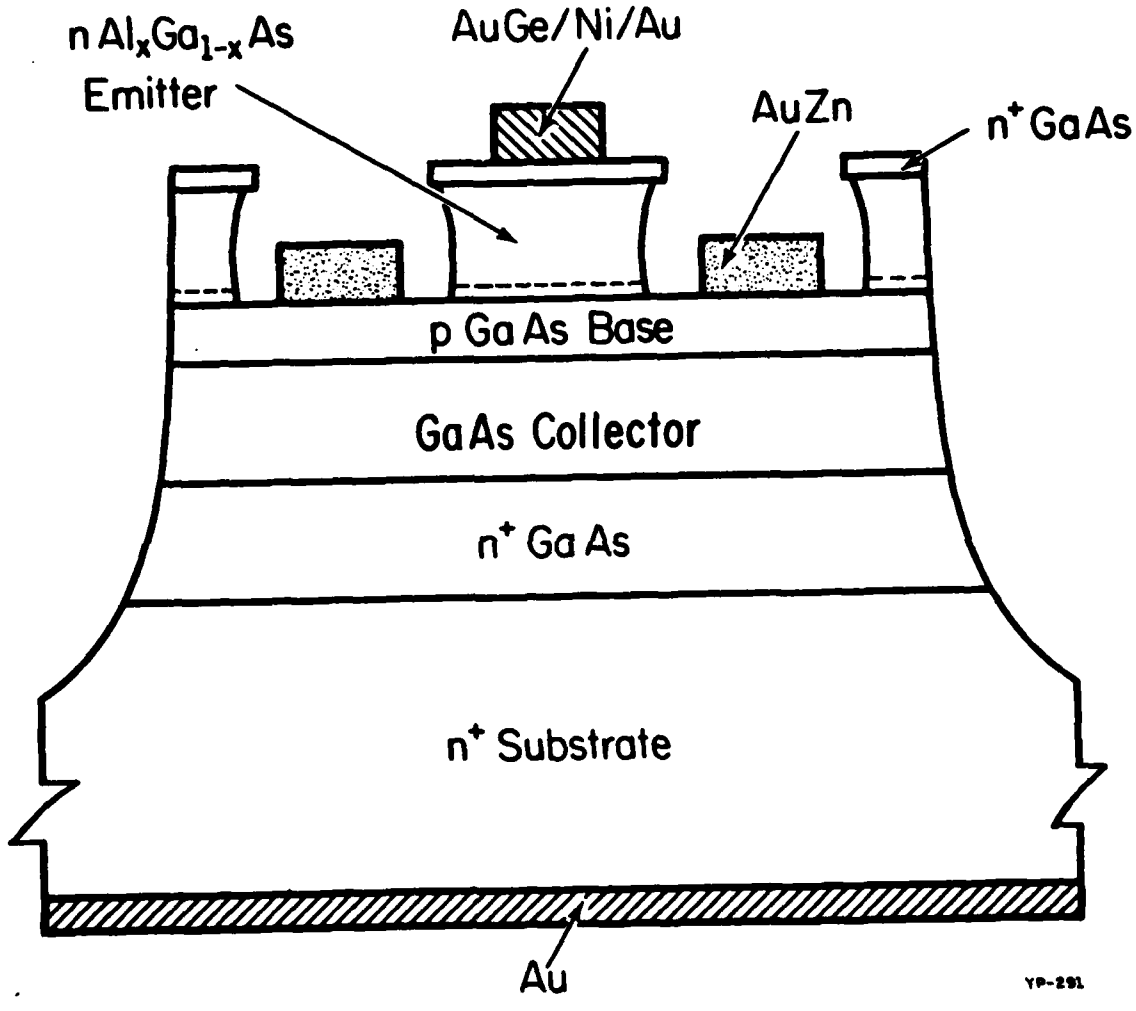


Figure 8 A Non-Inverted Heterojunction Bipolar Transistor

As compared to the inverted transistor fabricated by TI on materials prepared by the same MBE machine and same growth procedure, the non-inverted transistor showed at least a factor of 10 higher in current gain. This discrepancy could be caused by processing differences, in that the fabrication of non-inverted transistors only requires selective etches, while inverted transistors require ion implant and high temperature annealing. Consequently, the current gain of non-inverted transistors could simply reflect the property of an unperturbed heterojunction. On the other hand the MBE might also have unsymmetrical growth characteristics. It was reported from laser works[8] that when GaAs is grown on $Al_xGa_{1-x}As$ the interface always has higher trap density than the layers grown in reverse order. In short, such discrepancy indicates that further study of material properties relating to MBE growth conditions is essential to improve the current gain of an inverted heterojunction bipolar transistor.

C. HI^{2}L Gate Performance

Three types of basic HI^{2}L gate design were examined. They are designated as type A, B, and C design. The test bar layout containing these designs is shown in Figure 9, which also includes a family of test patterns and a prototype gate array using the type C gate design.

Of the three HI^{2}L gate designs, the one located at the top left corner (design A) used the most aggressive design rules. The circuits had practically zero yield. Design B, in the middle, used somewhat relaxed design rules. This design produced some good circuits, but the yield was generally low. Design C, shown at the top right corner, used the same design rules as design B, but has a two-sided base contact. The detail layout of gate design C is shown in Figure 10. The use of a two-sided base contact was originally intended to lower base spreading resistance of the transistor, but apparently it also has a positive effect on the yield. On a good slice better than 50% probe yield has been obtained from gate design C.

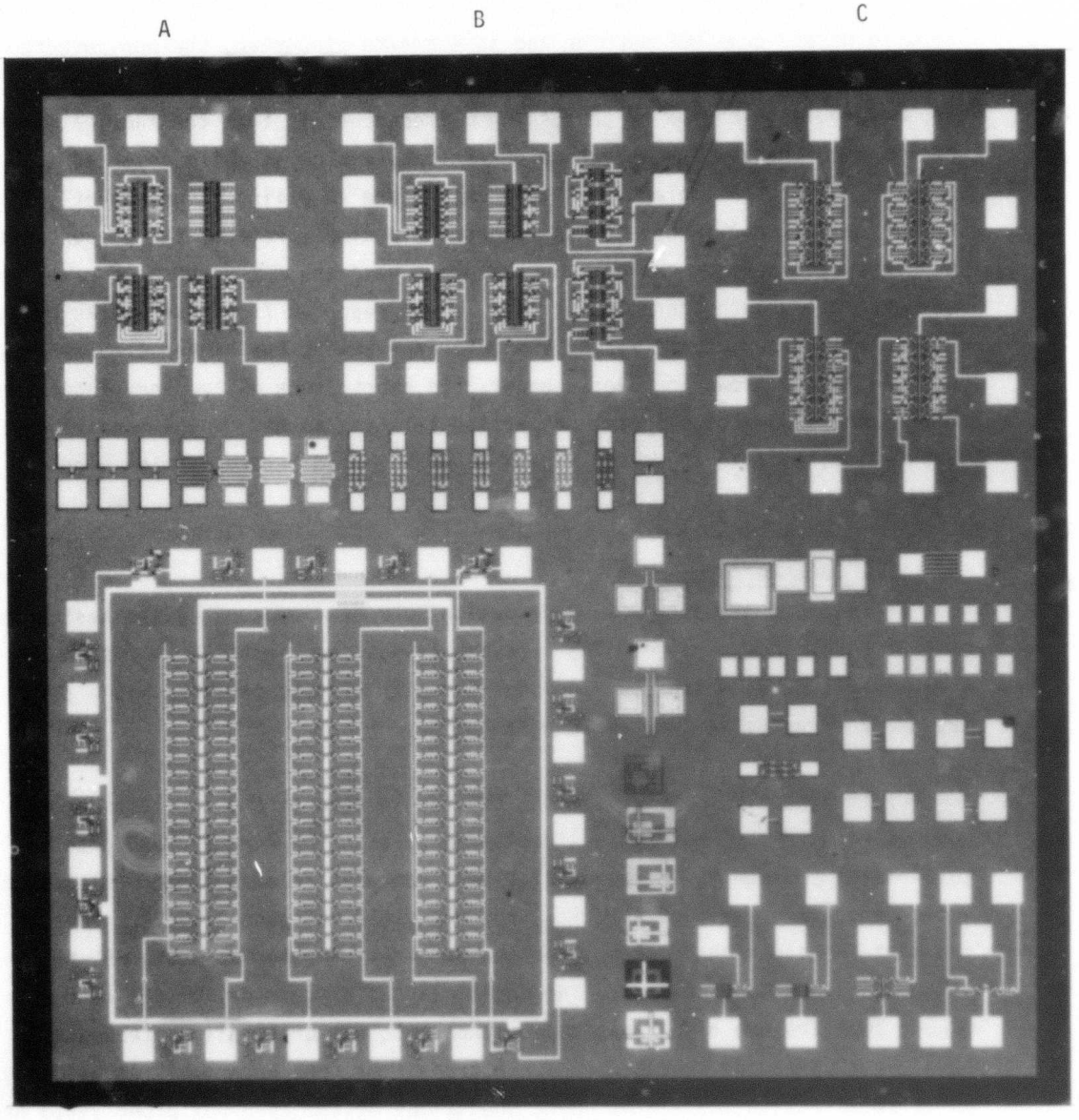


Figure 9 Micrograph of the Test Bar Layout

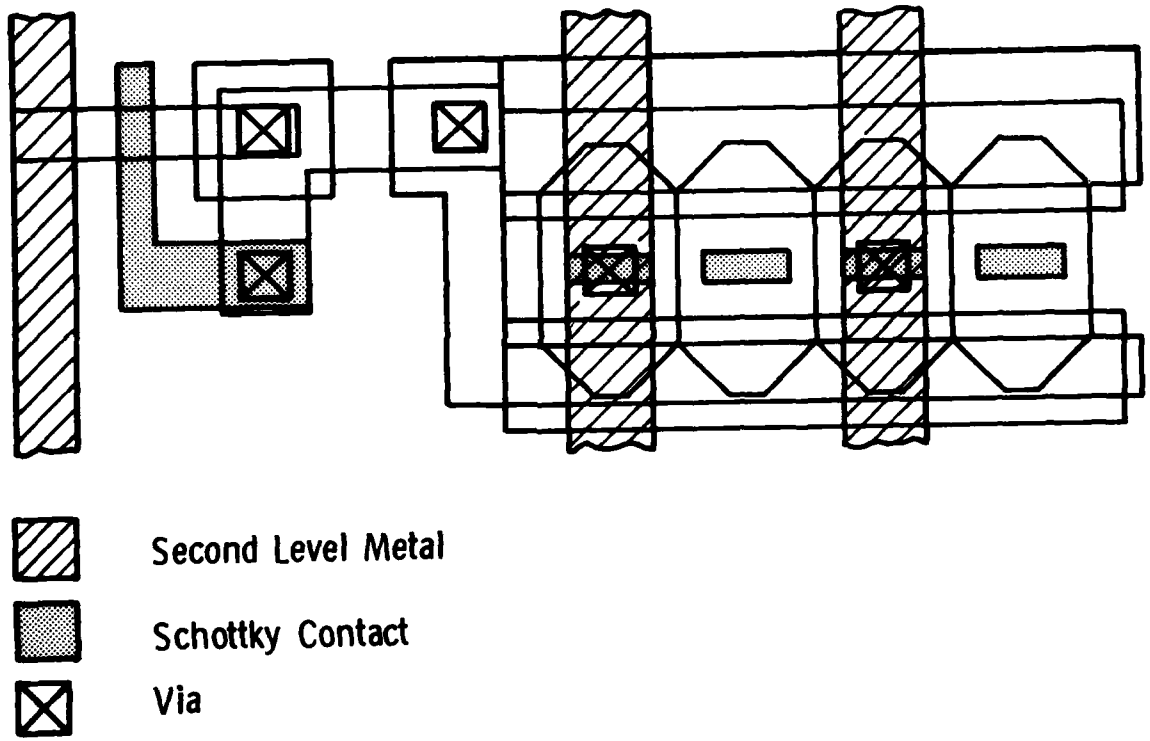


Figure 10 Layout of Gate Design C

The switching performance of the type C HI^2L gate was characterized by ring oscillator as well as by D-type divider circuit. Figure 11 shows the waveform of a 17-stage ring oscillator, which exhibits fully saturated switches with an expected logic high at 1.2 V and a logic low at 0.8 V. Figure 12 shows the measured HI^2L gate propagation delay vs power dissipation for fan-out of 1 and fan-out of 4. At V_{CC} = 2 V and power dissipation of 2.0 mW per stage the measured propagation delay from the ring oscillator is as low as 270 ps for fan-out of 1 and 470 ps for fan-out of 4. This compares rather favorably to the most advanced ECL gate arrays reported recently,[9] which have an average propagation delay of 0.83 ns and an average power dissipation of 0.54 mW per stage. More significantly, the HI^2L gate uses an area of only 1650 μm^2, while the ECL gate uses an area of 4620 μm^2, almost three times larger than the HI^2L.

Figure 13 shows the measured waveform of a divide-by-4 circuit, which was assembled in a ceramic 16-pin dual in-line package. The frequency divider was measured to a toggle frequency of 200 MHz. Since the frequency divider using D-type flip-flops has an average 4.5 gate delay, the toggle frequency corresponds to a gate delay approximately 1 ns per gate. Thus it is comparable to the value obtained from the ring oscillator. This confirms that integrated circuits fabricated using bipolar technology are far less load-sensitive than those using MESFET technology.

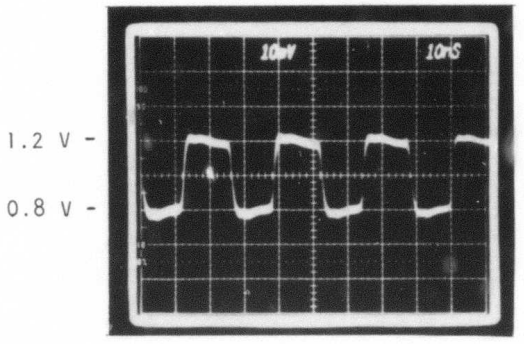


Figure 11 Waveform of 17-Stage Ring Oscillator. The probe used for this measurement has a 20X attenuation.

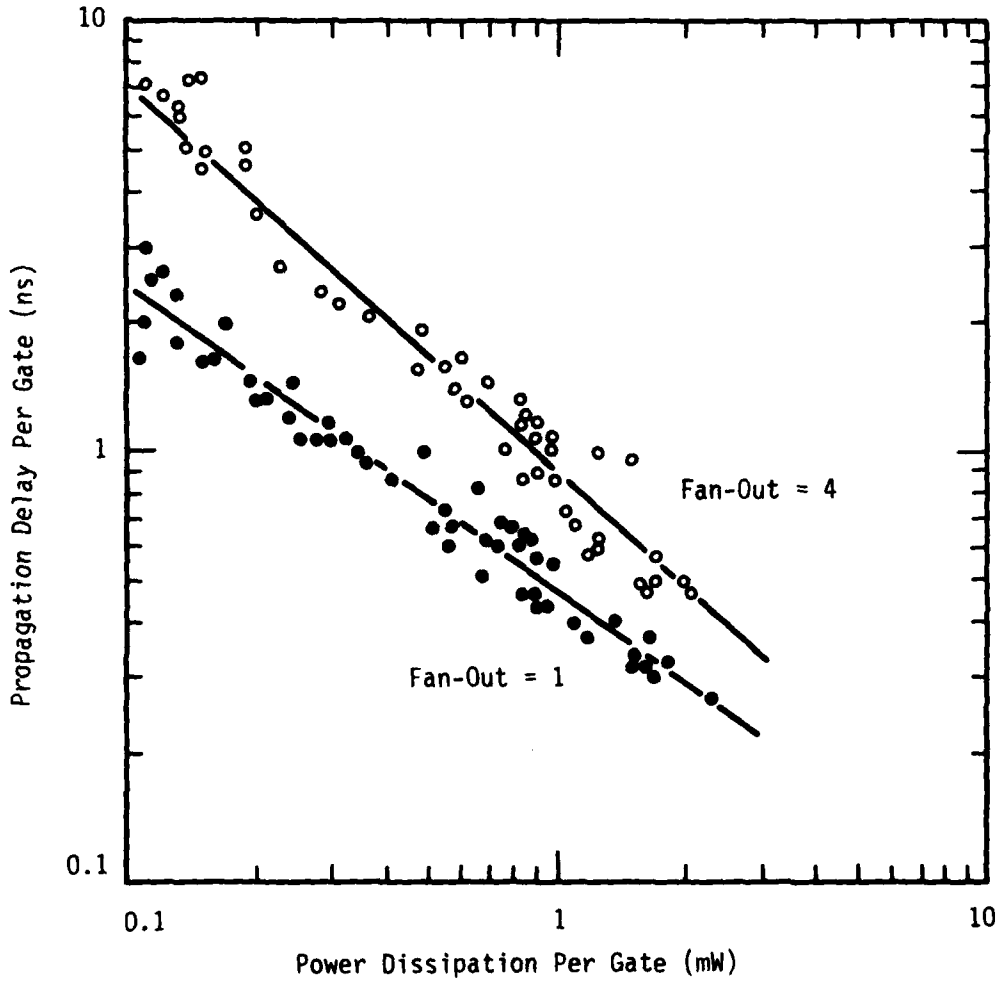


Figure 12 Measured HI^2L Gate Propagation Delay vs Power Dissipation

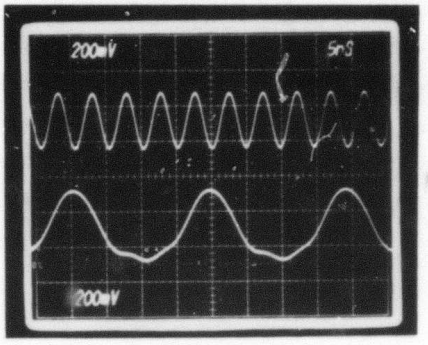


Figure 13 Measured Waveform of a Divide-by-4 HI^2L

SECTION IV
GATE ARRAY DESIGN

A. Prototype Gate Array

A prototype gate array with 114 internal gates and 25 I/O buffers and bonding pads was designed. A micrograph of the 1.25 x 1.25 mm^2 bar is shown in Figure 14. The prototype gate array uses type C basic gate design. It allows two wire channels between gates in the horizontal direction and a total of 13 wire channels between the columns of gates. The I/O buffer is a cluster of discrete transistors, FET loads, and Schottky diodes. These components can be joined together by interconnections and programmed to become either input or output buffers. Typical circuit schematics for input and output buffer designs are shown in Figure 15. The buffer design can be made compatible with 100K series ECL circuits or standard TTL circuits.

Figure 14, also shows that the prototype gate array was tested by simple inverter chains and ring oscillators. Three sets of such circuits, each composed of a 17-stage ring oscillator and a 19-stage inverter chain with fan-out of 1, 2, and 4 occupying the left, middle, and right column, were used in the test circuits. All internal gates in this test circuit share a common power supply pad; all I/O buffers share a different power supply pad. The use of two separate power supplies simplifies the diagnostic work for gate array circuit development.

Completely functional gate arrays, meaning that all ring oscillators and inverter chains are functional under one power supply, were made on several MBE wafers supplied by the University of Illinois. The measured propagation delay and power consumption per gate, in general, agrees with those measured by test patterns reported in previous sections.

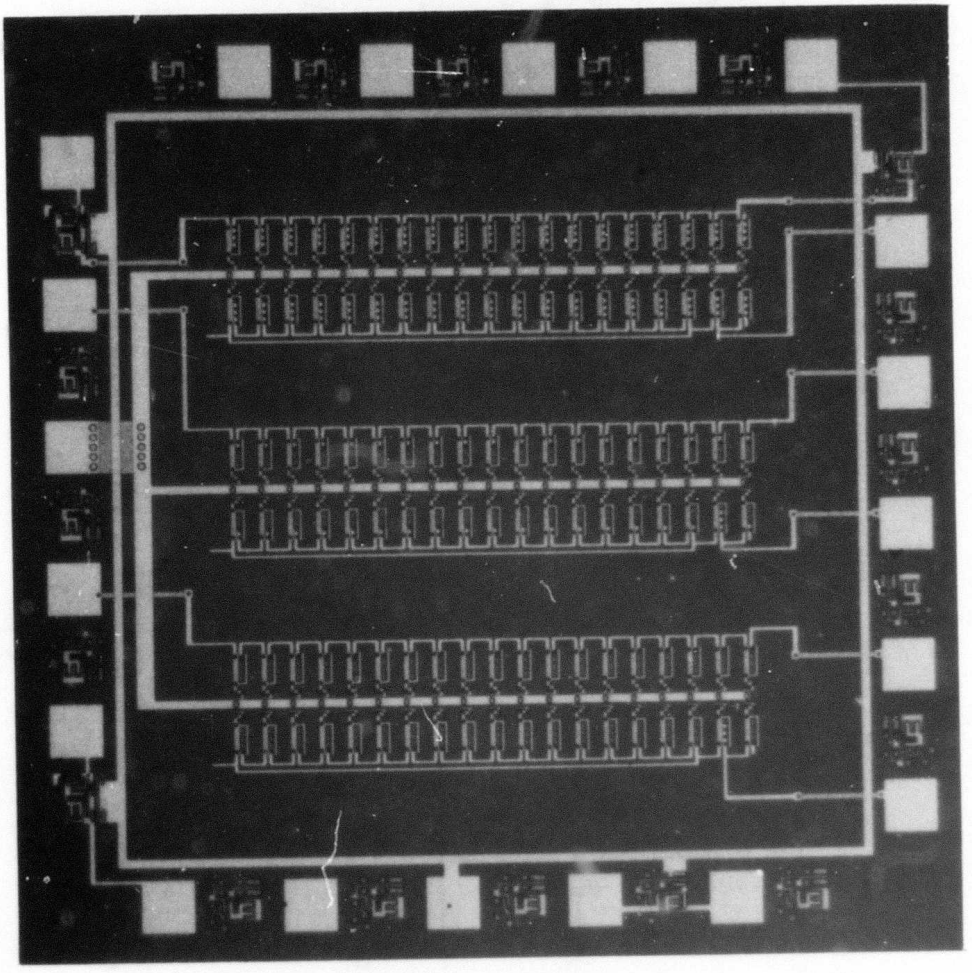
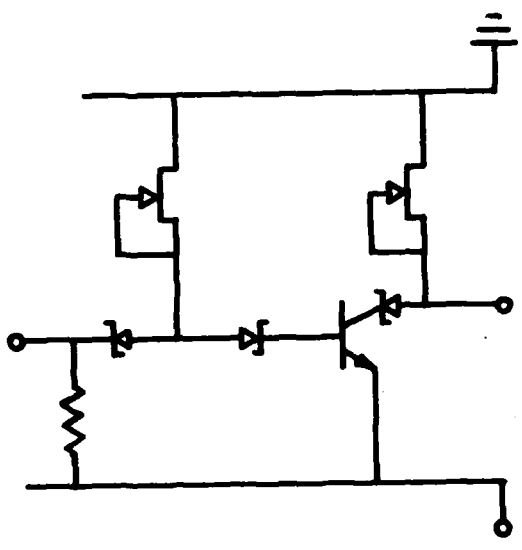


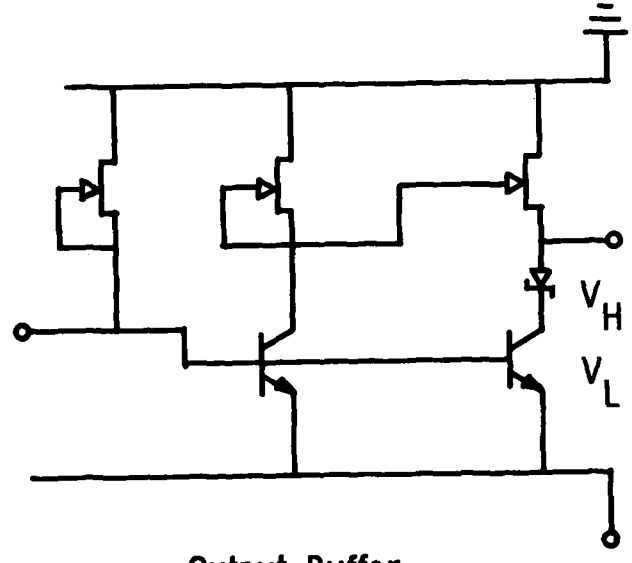
Figure 14 Micrograph of the Prototype Gate Array Design

I/O BUFFER DESIGN



Input Buffer

V_{EE} = -2.5 V



Output Buffer

V_{EE} = -2.5 V

V_{sat} = 0.2 V (MESFET)

V_{sat} = 0.1 V (Bipolar)

V_{SD} = 0.7 V (Schottky)

V_D = 1.2 V (Diode)

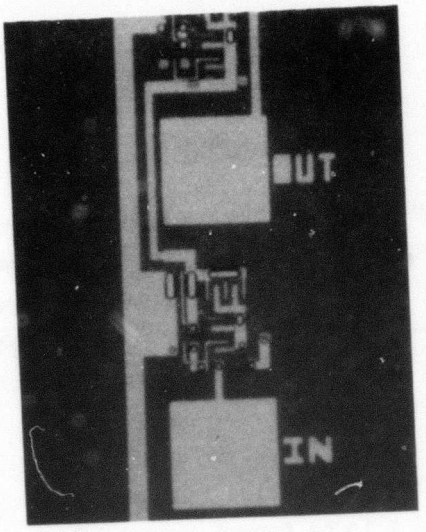
Figure 15 Circuit Schematics of Input and Output Buffers for the Prototype Gate Array

The I/O buffers were also successfully demonstrated. Figure 16(a) shows a micrograph of a test circuit consisting of an input buffer directly driving an output buffer. An oscilloscope photograph is shown in Figure 16(b) of the input and output waveforms for this circuit operating at a supply voltage of 2.5 V. The output signal in Figure 16(b) is of the same polarity as the input because it is inverted twice.

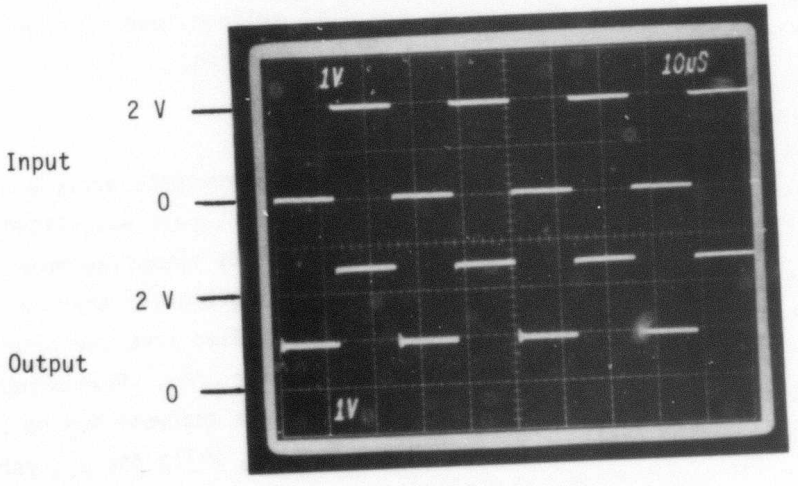
Preliminary characterization indicates that the input buffer requires a high voltage of 1.4 V to be turned on and a low voltage of 1.0 V to be turned off. These voltage levels would enable the input buffer to interface with TTL or ECL. In the latter case, a negative instead of positive supply voltage must be applied to the substrate and the V_{CC} power bus must be grounded. In the case of the output buffer, the output terminal was shown to be pulled to supply voltage when the output transistor was turned off, and to approximately 0.8 V when the output transistor was turned on. Such voltage levels may need modification if interface to standard TTL and ECL is required.

B. Divide-by-10/11 Prescaler

As a more realistic test circuit for the prototype gate array a pin-for-pin compatible GaAs equivalent to an off-the-shelf ECL part was, 11C90, designed. Figure 17 shows the circuit schematic and its operating modes. The design is a selectable divide-by-10 or divide-by-11 prescaler that in its ECL form is rated at 650 MHz. The circuit has been modified from the original NOR-gate design to the wired-AND gate design required for HI^2L. Preliminary division points are brought out in the event that failure analysis may be required. Moreover, this design utilizes a synchronous counter, while the ECL version is a combination of synchronous and asynchronous stages. The GaAs version has five gate delays in its feedback path and therefore has a projected maximum operating frequency of 1/(5 x gate delay). At gate delays of 500 ps this frequency would be 400 MHz. The power dissipated by the GaAs part is estimated to be 50 mW, while the ECL part requires 390 mW.



(a)



(b)

Figure 16(a) Micrograph of Cascade Input and Output Buffers, (b) Waveform at V_{CC} = 2.5 V

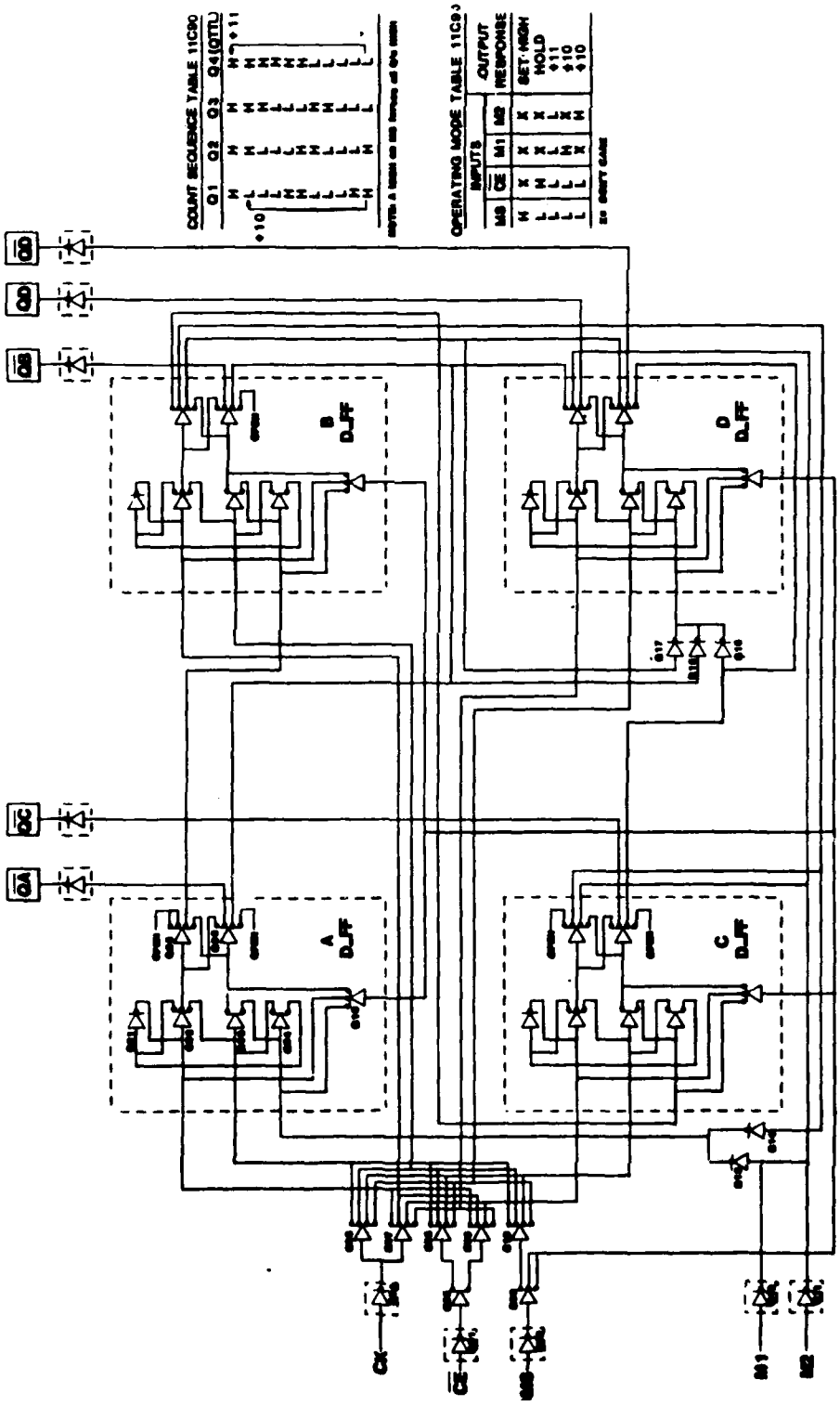


Figure 17 Circuit Schematic of Divide-by-10/11 Prescaler Design

This circuit has been simulated successfully using TI's Hardware Description Language (HDL) and Test Description Language (TDL) to verify the functionality of the design. These programs are part of TI's gate array development software systems and represent an initialization of a data base. In mature technologies, such as I^2L, STL, and CMOS, they are applied to simulate, partition, route interconnect, and generate photomasks. Many of these software programs share the same algorithms but they must be tailored specifically for each given technology. For the HI^2L gate array, fortunately, the software developed for either I^2L or STL was found to be transferable, making the task of circuit design using gate arrays relatively simple.

The circuit was laid out using a TI interactive graphics designer terminal (DT) employing a "macro-cell" approach to flip-flop stages and input and output gates. The interconnect used to create a flip-flop is stored as a design element on the DT and is retrieved and placed as needed. The design of the flip-flop is general-purpose; specific modifications for each stage of the counter have been made.

A micrograph of the completed circuit is shown in Figure 18. In the micrograph, the divide-by-10/11 circuit, which uses 44 internal gates, occupies the right center two-thirds of the gate array. And the left column is occupied by a 4-bit shift register design.

Several lots of materials, supplied primarily by the University of Illinois, with divide-by-10/11 circuit programmation were processed from August 1982 to January 1983. But no functional circuits were made. A number of problems have been identified.

As was discussed earlier, many of the materials obtained during this period had grown junction structures. The current gain of the transistor made from these materials is typically only $2 \sim 4$, which is considerably lower than current gain of 20 required by the circuit. On a few wafers with good current

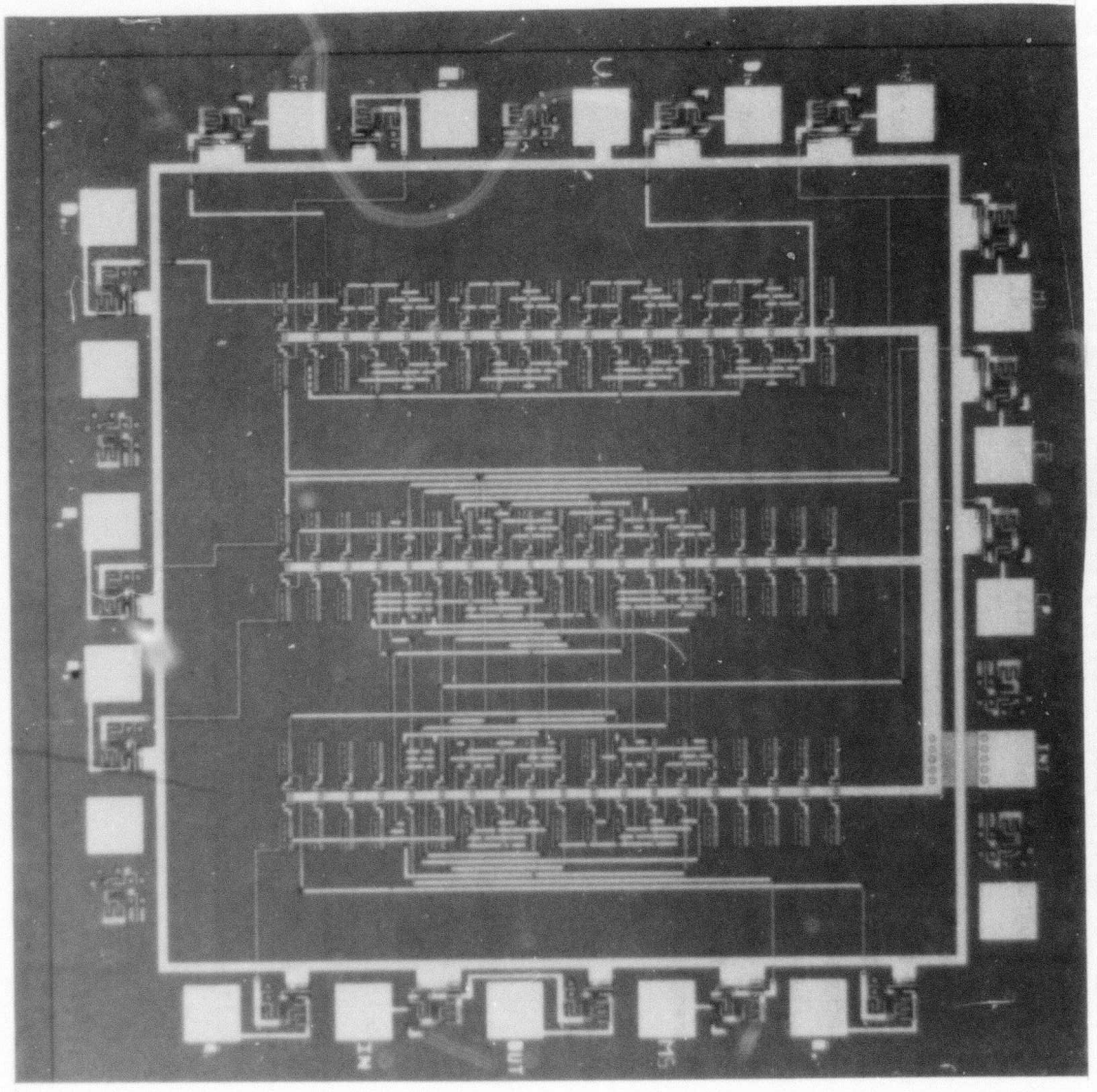


Figure 18 Micrograph of the Divide-by-10/11 Prescaler Design Using Prototype Gate Array

gain, however, the circuit yield was hampered by material uniformity and poor photolithography. Although material uniformity was largely solved by using in-house MBE wafers, photolithography enhancement has to wait until the establishment of an Optimetrix 10x DSW stepper. Thus at the end of the first year of this program, no finished circuits have yet been measured.

With partially functional circuits, however, we were able to identify several circuit design errors. Briefly, a parasitic p-n junction in parallel with the emitter base junction of the input buffer was uncovered. The junction acts as a shunt that prevents the input transistor from turning on by normal driving current. This was corrected by redesigning one level of photomask. A metal short between the power supply bus for internal gates and an input signal line from I/O buffer was also uncovered. This was corrected again by redesigning another photomask.

SECTION V
SUMMARY AND PLANS

During the first 12 months of the heterojunction bipolar gate array technology development program the primary objectives were to develop an epitaxial technique suitable for preparing uniform, submicron thickness AlGaAs/GaAs heterojunction layers on large diameter substrates, to establish a baseline process that enables the fabrication of large arrays of HI^2L gates, and to characterize npn transistor current gain in an inverted structure. Results of this work have shown that:

- MBE is superior to OM-CVD in preparing the required heterojunction materials.

- The baseline process is limited by the use of contact print, hence only small circuits with gate count less than 20 have been fabricated successfully.

- The current gain of an inverted transistor is considerably lower than that of a non-inverted transistor, and is more sensitive to epitaxial growth conditions.

Although progress was hampered by lack of sufficient materials and poor yield from fabrication, the measured results from good wafers did indicate that the HI^2L gate has well behaved logic levels, far less sensitive to load conditions, and has switching speed comparable to the best silicon ECL gates. With these encouraging results the tasks planned for the next 12 months of this program are:

- Improve MBE growth techniques and wafer handling procedures so that heterojunction layers on 2 inch wafers can be routinely produced.

- Conduct a systematic means to characterize material defects, aluminum composition, and trap density in MBE growth heterojunction materials.

- Establish the 10x DSW stepper centered photolithographic process.

- Complete computer aided design for gate array interconnection routing and design verification.

- Design and fabricate 1K and 4K gate arrays based HI^2L technology.

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